

WHAT IS CLAIMED IS :

1. A method for fabricating a semiconductor device comprising:
- forming a device isolation region on a semiconductor substrate to define a cell array region and a peripheral circuit region;
- forming a first gate in the cell array region, a second gate in the peripheral circuit region, and a third gate in the peripheral circuit region;
- implanting first impurity ions of a low concentration into a first portion of the semiconductor substrate adjacent to the second and third gates, using the second and third gates as a mask, to form a first impurity diffusion region of a first conductivity type;
- forming first gate spacers on lateral sides of the first, second, and third gates;
- implanting second impurity ions of a low concentration into a second portion of the semiconductor substrate adjacent to the first gate and first gate spacers, using the first gate and first gate spacers as a mask, to form a second impurity diffusion region of a first conductivity type;
- implanting third impurity ions of a low concentration into a third portion of the semiconductor substrate adjacent to the third gate and first gate spacers, using the third gate and first gate spacers as a mask, to form a third impurity diffusion region of a second conductivity type;
- forming an insulating layer over the semiconductor substrate, first through third gates, and first gate spacers;

20 etching the insulating layer in the peripheral region to form second gate spacers
21 adjacent to the first spacers adjacent to the second and third gates;
22 implanting fourth impurity ions of a high concentration into a fourth portion of the
23 semiconductor substrate adjacent to the second gate and second spacers, using the second
24 gate and first and second spacers as a mask, to form a fourth impurity diffusion region of
25 a first conductivity type; and
26 implanting fifth impurity ions of a high concentration into a fifth portion of the
27 semiconductor substrate adjacent to the third gate and second spacers, using the third gate
28 and first and second spacers as a mask, to form a fifth impurity diffusion region of a
29 second conductivity type.

1 2. A method for fabricating a semiconductor device, as recited in claim 1, wherein
2 the first conductivity type is n-type.

4 3. A method for fabricating a semiconductor device, as recited in claim 1, wherein
5 the implanting of first impurity ions has a lower ion diffusivity than the step of implanting
6 second impurity ions.

1 4. A method for fabricating a semiconductor device, as recited in claim 1, wherein
2 the first through third gates comprise polysilicon.

5. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of first impurity ions is performed using arsenic with a dose range of about 5×10^{12} ions/cm² and at an energy range of about 50 keV.

6. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of second impurity ions is performed using phosphorous with a dose range of about 5×10^{12} ions/cm² and at an energy range of about 30 keV.

7. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of third impurity ions is performed using boron or BF_3 with a dose range of about 1×10^{13} ions/cm² and at an energy range of about 20 keV.

8. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of fourth impurity ions is performed using arsenic with a dose range of about 5×10^{15} ions/cm² and at an energy range of about 50 keV.

9. A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of fifth impurity ions is performed using boron or BF_3 with a dose range of about 5×10^{15} ions/cm² and at an energy range of about 20 keV.

1 10. A method for fabricating a semiconductor device, as recited in claim 1, further
2 comprising:

3 forming a silicide layer over the semiconductor substrate, the second gate, and the
4 third gate in the peripheral circuit region; and

5 forming an interlayer insulating layer over the substrate and first through third
6 gates;

7 etching a selected portion of the interlayer insulating layer in the cell array region,
8 using the insulating layer as for an etching stopper, and forming a contact opening
9 adjacent to the first gate.

1 11. A method for fabricating a semiconductor device, as recited in claim 10,
2 wherein the forming of a silicide layer is further comprises

3 forming a transition metal over the substrate and the second and third gates

4 annealing the substrate and the transition metal to form the silicide layer.

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1 12. A method for fabricating a semiconductor device, as recited in claim 11,
2 wherein during the annealing of the substrate and the transition metal, the first through
3 fifth impurities are diffused into the first through fifth impurity diffusion regions,
4 respectively.

1 13. A method for fabricating a semiconductor device, as recited in claim 10,
 2 wherein the a remaining portion of the insulating layer, after the etching of the insulating
 3 layer in the peripheral region, serves as a barrier layer to prevent silicidation in the cell
 4 array area during the forming of a silicide layer.

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 1 14. A method for fabricating a semiconductor device, as recited in claim 10,
 2 wherein the interlayer insulating layer has a first etching rate at least five times as high as
 3 a second etching rate of the insulating layer.

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 1 15. A method for fabricating a MOS transistor in a semiconductor device, the
 2 method comprising the steps of:
 3 forming a gate electrode over a semiconductor substrate;
 4 implanting first impurity ions at a low concentration of a first conductivity type,
 5 using the gate electrode as a mask, to form a first impurity diffusion layer;
 6 forming first spacers on lateral sides of the gate;
 7 implanting second impurity ions at a low concentration of a second conductivity
 8 type, using the gate and first spacers as a mask, to form a second impurity diffusion layer;
 9 forming a second spacers adjacent to the first spacers;
 10 implanting third impurity ions of high concentration of a second conductivity type,
 11 using the gate and the first and second spacers as a mask, to form a third impurity
 12 diffusion layer; and

annealing and diffusing the impurity diffusion layers to overlap the first diffusion layer with the second diffusion layer.

16. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the first conductivity type is n-type.

17. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of first impurity ions is performed using arsenic with a dose range of about 5×10^{12} ions/cm² and at an energy range of about 50 keV.

18. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of second impurity ions is performed using boron or BF₃ with a dose range of about 1×10^{13} ions/cm² and at an energy range of about 20 keV.

19. A method for fabricating a MOS transistor in a semiconductor device, as recited in claim 15, wherein the implanting of third impurity ions is performed using boron or BF₃ with a dose range of about 5×10^{15} ions/cm² and at an energy range of about 20 keV.